REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 10/6/05, Applicant is filing this amendment. Claims 1-20 are pending.

In the Office Action mailed 10/6/05, the Examiner has rejected claims 1-5, 9-12, 16 and 17 under 35 U.S.C. §102(e) as being anticipated by Nobunaga (U.S. Pub. No. 2005/0005183 A1). In reply, Applicant has amended independent claims 1, 9 and 16 to recite that the strobe selected is to allow a data transfer at a bit transfer rate of a data source (such as the recited memory in claim 9). The clock signals (CLK_STD and CLK_FDA) disclosed in Nobunaga may clock the data at two different clock rates, but the one clock (CLK_STD) is used in a standard mode and the second clock (CLK_FDA) is used in a fast data access mode (paragraphs [0029-0030] of Nobunaga). The different clock frequencies are used to switch the memory device from its standard operating mode to a fast data access mode (paragraphs [0067] of Nobunaga). However, Nobunaga does not disclose the selecting of strobes to accommodate different data sources (such as memory) that have different bit transfer rate per strobe, as now clearly recited in the independent claims.

Accordingly, Applicant submits that the amended claims overcome the Examiner's rejection based on Nobunaga and respectfully requests the Examiner to withdraw the 35 U.S.C. §102(e) rejection

Furthermore, Applicant has amended claim 16 to replace "probes" with "strobes" and, therefore, requests the Examiner to withdraw the claim objection as well.

Finally, in reference to the Examiner's comments on priority, the present application seeks priority to a domestic application (not foreign priority as noted by the Examiner). Furthermore, the present application is a continuation-in-part application basing priority to application 10/269,912. Thus, new matter may be introduced in the present application, while a claim for priority to the parent may be sought for material that is also disclosed in the parent.

Application 10/269,912 clearly shows the use of a data buffer in a memory controller 14, which is coupled to a memory system 24 (see Fig. 2 of 10/269,912).

Furthermore, Figure 5 of 10/269,912 also shows data buffer 48 coupled to memory channels. The data pathway from the memory channels are also shown in Figure 6 of 10/269,912. Accordingly, Applicant submits that the claim for priority is appropriate, at least for matter in the present application that is also disclosed in application 10/269,912.

Accordingly, Applicant submits that the present application is in condition for allowance and requests the Examiner to allow pending claims 1-20, as amended.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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